



Substitute for form 1449A/PTO

*(use as many sheets as necessary)*

Sheet	1	of	2
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Application Number	09/448,884
Filing Date	November 24, 1999
First Named Inventor	Sharp, Joelle
Art Unit	2818
Examiner Name	David Vu
Attorney Docket Number	018865-003600US

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Frühling

07/19/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Kind Codes of U.S. Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.



<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		<b>Complete If Known</b>			
		Application Number	09/448,884		
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Sheet	2	of	2	Attorney Docket Number	018865-003600US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
DV	0005	CHANG et al., "A Highly Manufacturable Corner Rounding Solution for 0.18 $\mu$ m Shallow Trench Isolation," IEDM Tech. Digest, pp. 661-664 (1997).	
	0006	NOURI et al., "An Optimized Shallow Trench Isolation for sub-0.18 $\mu$ m ASIC Technologies," SPIE Vol. 3506, pp. 156- 166 (September 1998).	
	0007	MATSUDA et al., "Novel Corner Rounding Process for Shallow Trench Isolation utilizing MSTs (Micro-Structure Transformation of Silicon)," IEDM Tech. Digest, pp. 137-140 (December 1998).	
DV	0008	NANDAKUMAR et al., "Shallow Trench Isolation for advanced ULSI CMOS Technologies," IEDM Tech. Digest, pp. 133-136 (December 1998).	

Examiner Signature	<i>gheland</i>	Date Considered	07/19/04
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**Complete if Known**

<b>Application Number</b>	<b>09/448,884</b>
<b>Filing Date</b>	<b>November 24, 1999</b>
<b>First Named Inventor</b>	<b>Joelle Sharp, et al.</b>
<b>Group Art Unit</b>	<b>2811</b>
<b>Examiner Name</b>	<b>Unassigned</b>
<b>Attorney Docket Number</b>	<b>018865003600</b>

**(use as many sheets as necessary)**

Sheet 2 of 2

**OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS**

[illegible]

**Examiner  
Signature**

Hubbard

Date Considered

08/03/04.

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